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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,766	05/18/2006	Takamitsu Yamada	R2184.0495/P495	3580

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/579,766	YAMADA, TAKAMITSU	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/18/06;5/27/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/579,766 filed on 5/18/06.

Claims 1-15 remain pending in the application.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1 and 9 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed invention lacks patentable utility. Claims 1 and 9 a data structure per see without patentable utility. Claim 7 is non-statutory subject matter because a program without storing in a physical storage device executed by a computer processor, and excluding all kind carrier waves is non-statutory subject matter.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-15 is rejected under 35 U.S.C. 102(e) as being anticipated by Hekmatpour et al. (7,313,772 B2).

6. As to claims 1 and 9, Hekmatpour et al. teach an assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit,

comprising: a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations (examples are a design; design constructs; designs blocks shown in Fig. 2; assertion schemas stored in a database shown in Fig. 1; Fig. 10); a first storing unit that stores the design data generated by the specification inputting unit (examples are a design; design constructs; designs blocks shown in Fig. 2; Fig. 1, 10); a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data (example are assertion schemas stored in a database shown in Fig. 1; 10); a second storing unit that stores the property generated by the property generating unit (example are assertion schemas stored in a database shown in Fig. 1; Fig. 4, 10 and its description); and an assertion generating unit that converts the property into an assertion description by reading the property generated by the property generating unit from the second storing unit (Fig. 1; assertion generator may embed the assertions in the design HDL or provide them in a separate design module), wherein the property

generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data (at least see col. 9 lines 6-41; Fig. 1, 5 and its description).

7. As to claims 2 and 10, Hekmatpour et al. teach, wherein the property generating unit generates at least one or more properties, and the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations (Fig. 10).

8. As to claims 3 and 11, Hekmatpour et al. teach, wherein the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property (Fig. 10, 11).

9. As to claims 4 and 12, Hekmatpour et al. teach, wherein the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property (Fig. 2, 10).

10. As to claims 5 and 13, Hekmatpour et al. teach, wherein the assertion generating unit converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or

a signal name or a state name in the logic table or the state table edited by the specification inputting unit is added, and the property is the temporal property (Fig. 2, 10).

11. As to claims 6 and 14, Hekmatpour et al. teach, wherein the specification inputting unit is a business tool of spread sheet software and expands the design data into a graphic structure and inputs the graphic structure in the first storing unit (Fig. 1 shows a database; Fig. 2 shows design data; Fig. 10 shows assertion generation system).

12. As to claim 7, Hekmatpour et al. teach a program that makes a computer function as the units of the assertion generating system as claimed in claim 1 (Fig. 3-9 show a program).

13. As to claim 8, Hekmatpour et al. teach a circuit verifying system, comprising: the assertion generating system as claimed in claim 1, wherein the circuit verifying system executes assertion verification of a semiconductor integrated circuit by using the assertion description generated by the assertion generating system (Fig. 1, 10 and 11 show assertion system).

14. As to claim 15, Hekmatpour et al. teach a manufacturing method of a semiconductor device, comprising: a designing step that designs an integrated circuit having a predetermined function ; a simulating step that simulates the integrated circuit by using the assertion generated at the assertion generating method as claimed in claim 9; and a manufacturing step that manufactures a semiconductor device based on specifications of the integrated circuit, wherein the semiconductor device in which

design meeting specifications is confirmed is manufactured by that the integrated circuit is simulated by the assertion obtained at the assertion generating method as claimed in claim 9 (see claim 1 and 9 rejection; the limitations are known to be inherently in the art).

15. Claims 1-15 is rejected under 35 U.S.C. 102(e) as being anticipated by Mitra et al. (7,325,209 B2).

16. As to claims 1 and 9, Mitra et al. teach an assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit (see abstract, summary, Fig. 1-4), comprising: a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations (HDL design; Fig. 4); a first storing unit that stores the design data generated by the specification inputting unit (Fig. 4); a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data (Fig. 4); a second storing unit that stores the property generated by the property generating unit (Fig. 4); and an assertion generating unit that converts the property into an assertion description by reading the property generated by the property generating unit from the second storing unit (Fig. 4; translator or transformer), wherein the property generated by the property generating

unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data (Fig. 2-4).

17. As to claims 2 and 10, Mitra et al. teach, wherein the property generating unit generates at least one or more properties, and the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations (Fig. 1, 4).

18. As to claims 3 and 11, Mitra et al. teach, wherein the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property (Fig. 2-4).

19. As to claims 4 and 12, Mitra et al. teach, wherein the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property (Fig. 1-4).

20. As to claims 5 and 13, Mitra et al. teach, wherein the assertion generating unit converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or

a signal name or a state name in the logic table or the state table edited by the specification inputting unit is added, and the property is the temporal property (Fig. 1-4).

21. As to claims 6 and 14, Mitra et al. teach, wherein the specification inputting unit is a business tool of spread sheet software (known art) and expands the design data into a graphic structure and inputs the graphic structure in the first storing unit (Fig. 1-4).

22. As to claim 7, Mitra et al. teach a program that makes a computer function as the units of the assertion generating system as claimed in claim 1 (Fig. 1-4).

23. As to claim 8, Mitra et al. teach a circuit verifying system, comprising: the assertion generating system as claimed in claim 1, wherein the circuit verifying system executes assertion verification of a semiconductor integrated circuit by using the assertion description generated by the assertion generating system (Fig. 1-4).

24. As to claim 15, Mitra et al. teach a manufacturing method of a semiconductor device, comprising: a designing step that designs an integrated circuit having a predetermined function ; a simulating step that simulates the integrated circuit by using the assertion generated at the assertion generating method as claimed in claim 9; and a manufacturing step that manufactures a semiconductor device based on specifications of the integrated circuit, wherein the semiconductor device in which design meeting specifications is confirmed is manufactured by that the integrated circuit is simulated by the assertion obtained at the assertion generating method as claimed in claim 9 (Fig. 1-4; the limitations are known to be inherently in the art).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, A.U. 2825